APPLICATION NOTE

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Design guidelines for COG modules with Philips monochrome LCD drivers

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SCOPE OF THIS APPLICATION NOTE

The purpose of this application note is to explain how to design optimal ITO layout on the input side of the LCD driver IC. The design guidelines in this Application Note apply to all Philips monochrome LCD driver ICs unless clearly stated otherwise. If correctly followed, these guidelines will help toward successful first time module design and better overall display performance.

WHO SHOULD READ THIS APPLICATION NOTE?

It is important that this application note is read by the engineers in charge of the LCD module design and ITO layout design on the interface side. Both module maker and OEM (setmaker) should find this application note useful.

DISCLAIMER	While all reasonable efforts are undertaken to ensure that the information contained within this Application Note is up to date and correct, Philips Semiconductors will accept no liability for errors or omissions resulting in loss of time and/or monetary investment.

ITO LAYOUT GUIDELINES FOR COG MODULES WITH PHILIPS LCD DRIVER ICS

GUIDELINES FOR POWER SUPPLY LINES V_{SS}, V_{DD}, V_{LCD}.

In COG applications the resistance of ITO tracks may not be neglected. Special attention must be paid to ITO layout in order that the effects of track resistance are minimised to an acceptable level.

Specifically with COG applications in mind, Philips LCD driver ICs' power supply circuits are separated internally into V_{DD1}, V_{DD2}, V_{DD3}, V_{SS1}, V_{SS2} supply rails. This is done in order that the module maker can connect these supply circuits via separate ITO tracks. In this way the common (shared) part of the ITO track is minimised or eliminated, thus reducing the amount of common-mode electrical noise.

For similar reasons, the LC drive supply circuits are separated internally into V_{LCDIN}, V_{LCDOUT}, $V_{LCDSENSE}$. The part of the ITO supply track that is shared by these circuits must be kept to a minimum.

Fig.1 and Fig.2 represent schematically the ITO & glass-to-PCB connection paths in two typical configurations. Suggested maximum resistance values of the power supply for a typical small display application (pixel size approx. 0.25 x 0.25 mm^2) are given in Table 1. **These limits are heavily dependent on display load and may have to be revised for a particular application**. Excessive track resistance, especially common (shared) track and connection resistance, may result in deterioration of display quality, increased power consumption and/or incorrect operation.

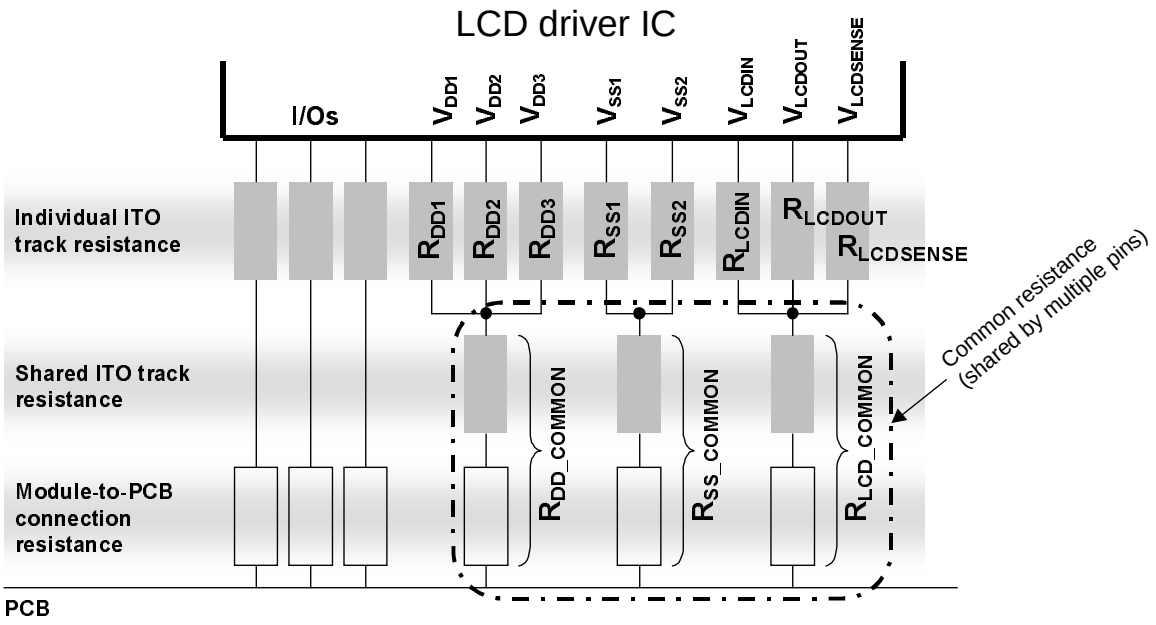

Fig.1 $V_{DD1} = V_{DD2,3}$

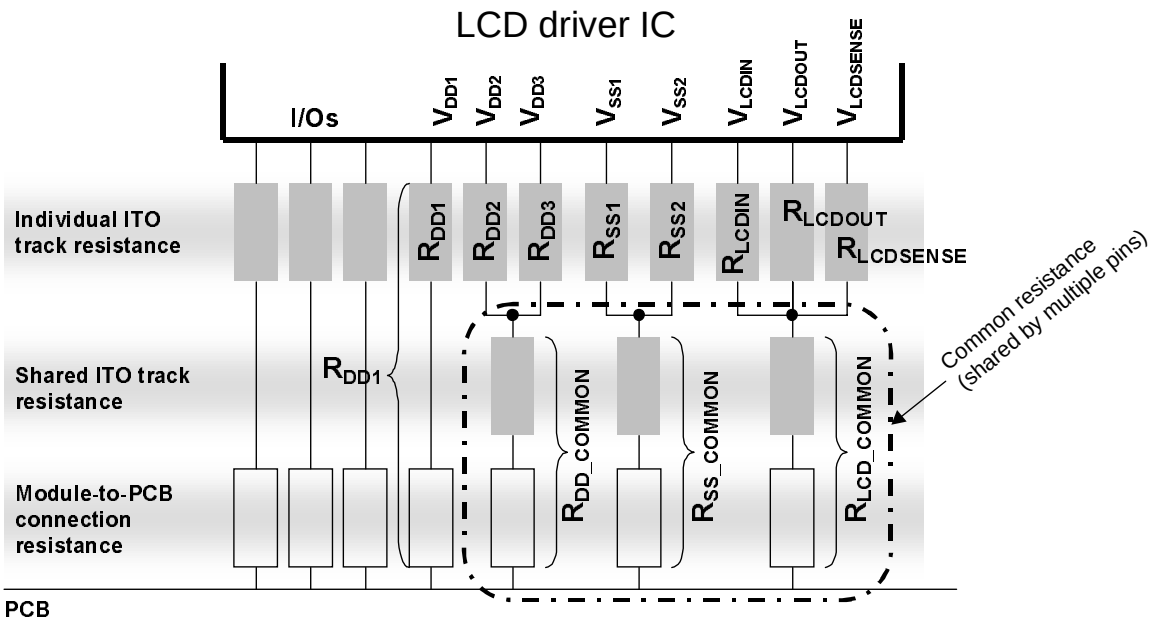

Fig.2 $V_{DD1} \neq V_{DD2,3}$

Table 1 Suggested maximum ITO track resistance.

RESISTANCE PATH	description	max resistance, Ω
R_{DD_COMMON}	common V_{DD} track (incl. connector)	40*
R_{DD1}	positive logic supply	500
R_{DD2}	positive charge pump supply	200
R_{DD3}	positive analogue supply	2k
R_{SS_COMMON}	common V_{SS} track (incl. connector)	40*
R_{SS1}	negative supply (excl. charge pump)	80
R_{SS2}	negative charge pump supply	200
R_{LCD_COMMON}	common V_{LCD} track (incl. connector)	60*
R_{LCDOUT}	generated output V_{LCD}	100
R_{LCDIN}	V_{LCD} input to chip	500
$R_{LCDSENSE}$	V_{LCD} sense input	2k

* NOTE: common-mode resistance in the supply circuits is by far the most critical element for display optical performance. It is most effectively minimised by connecting the separate ITO tracks outside of the LCD glass (on PCB, FPC, foil etc) instead of at the connection point on the glass ledge. However this may not always be practical in the application.

HINT: in order to keep the ITO track resistance to a minimum, the pitch and position of the module connection to the outside should be selected such that the power tracks run as straight as possible to the glass edge. In order to minimise common connection resistance, use low-ohmic elastomeric connection, metal pin connection or ACF bonded flat cable.

Fig.3 shows an example of how the ITO layout for the power supply tracks may look in practice.

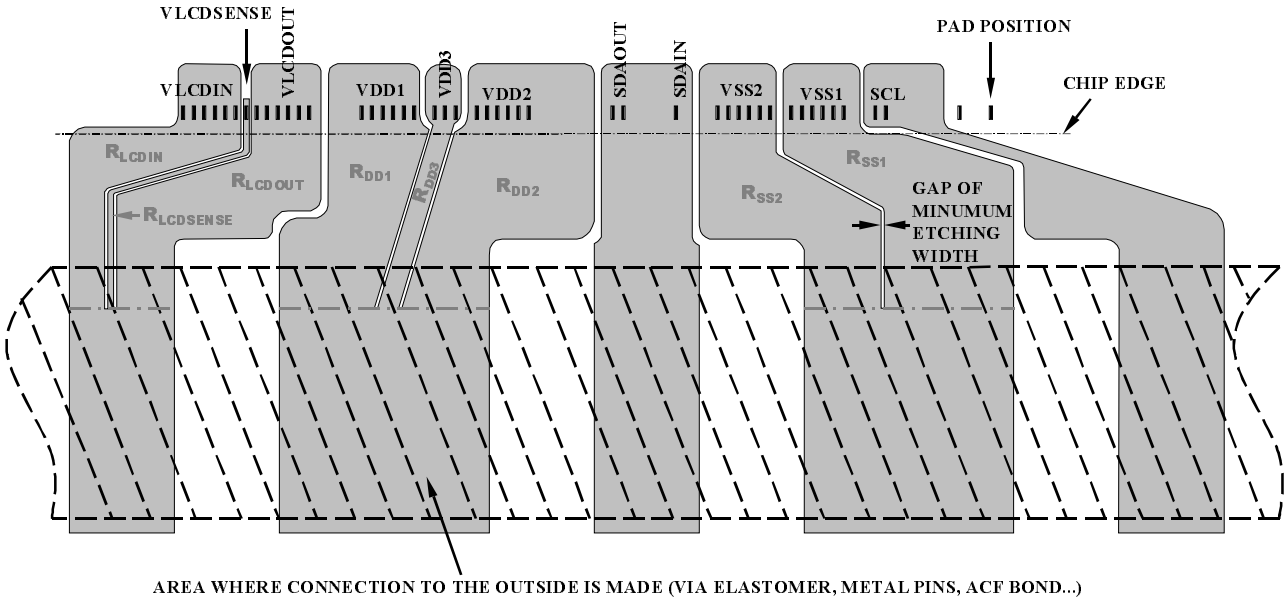

Fig.3 Example ITO layout for V_{SS}, V_{DD}, V_{LCD}.

EXCEPTIONS FROM THE GENERAL RULE: OM6208, OM6211, OM6213, OM6215, OM6217, PCF8811, PCF8813, PCF8814.

In the LCD driver types that are listed above a slightly different power architecture is implemented where the V_{LCD} voltage generation is concerned. Because of this the ITO layout guidelines for connecting pins V_{LCDIN}, V_{LCDOUT}, $V_{LCDSENSE}$ are also different. Please refer to Table 2 below.

Table 2

RESISTANCE PATH	description	max resistance, Ω
R_{LCD_COMMON}	common V_{LCD} track (incl. connector)	60
R_{LCDOUT}	generated output V_{LCD}	0
R_{LCDIN}	V_{LCD} input to chip	0
$R_{LCDSENSE}$	V_{LCD} sense input	0

In practice this means that V_{LCDIN}, V_{LCDOUT}, $V_{LCDSENSE}$ should be connected together with one thick ITO track.

GUIDELINES FOR I/O LINES

AC characteristics of the I/O lines are also affected by the ITO track impedance. The ITO track resistance together with any parasitic capasitances will add RC-type delay constants, which should be taken into account. It is recommended that COG modules are not operated close to the limits of the interface timing requirements. Particular attention must also be paid to open-drain outputs (see the next section “GUIDELINES FOR I²C-BUS PINS SDA, SCL”).

GUIDELINES FOR I²C-BUS PINS SDA, SCL

The SDA line in I²C devices is an open-drain output and therefore needs an external pull-up resistor. The ITO track resistance R_{ITO}, forms a potential divider together with the pull-up resistor $R_{PULL-UP}$. Because of this there is a danger that the the other device(s) on I²C-bus will not see a valid logic LOW level when the SDA line is driven LOW by the LCD driver IC, e.g. during the ACKnowledge cycle or during read-back from the IC. This is illustrated in Fig.4.

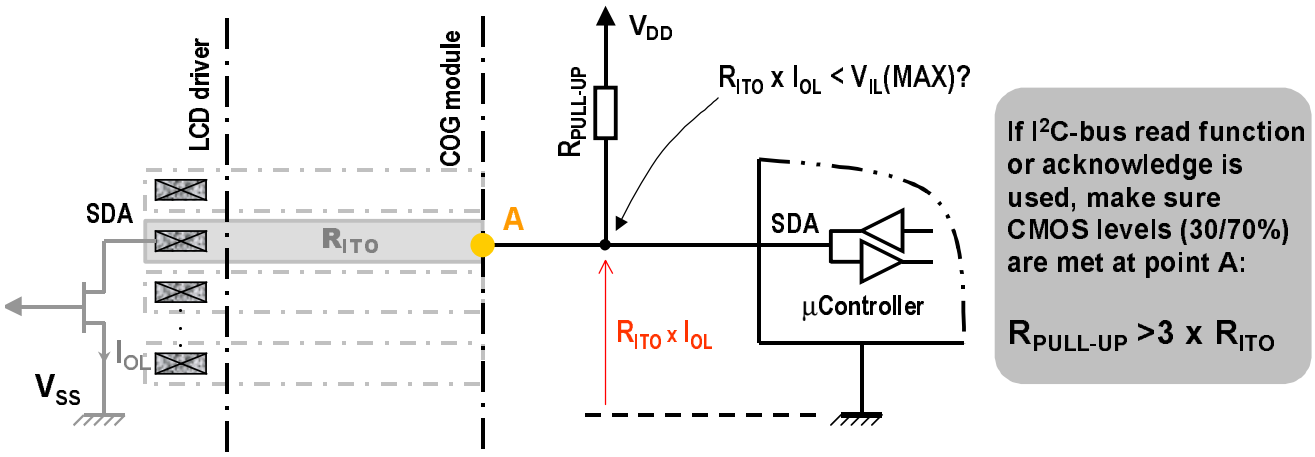

Fig.4 Effect of ITO resistance in the SDA line.

For this reason the SDA signal in LCD driver ICs is sometimes split into SDAIN and SDAOUT. A number of possibilities for connecting LCD to the host micro exist then, three of which are illustrated here:

1) The I²C protocol is fully implemented in the system, i.e. the master-transmitter device (host microcontroller) expects an ACKnowledge after each byte. In this case connect LCD driver's SDAIN and SDAOUT pins on glass with a single ITO trace, taking care to minimise track and connection resistance. Choose pull-up resistor value that will ensure V_{IL} specification of the other device(s) on the I²C-bus is always met, under all conditions and including all tolerances. Note that the value of $R_{PULL-UP}$ directly affects the SDA signal rise time. Take care that $R_{PULL-UP}$ is not so high that the maximum rise time limit is violated. A simple rule in this case is to make sure that $2C_{SDA} \times R_{PULL-UP} < t_R(max)$, where C_{SDA} is the capacitance of SDA bus rail including associated parasitic pad capacitances of all devices connected to the I²C-bus and $t_R(max)$ is the specified maximum rise time.

This configuration is shown in Fig.5.

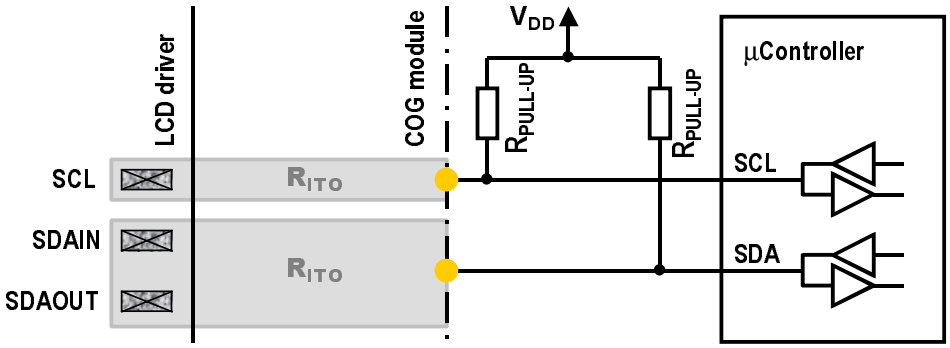

Fig.5 Typical configuration: direct connection to microcontroller.

2) The I²C protocol is fully implemented in the system but the value of pull-up resistor that is required to satisfy the *maximum logic low level* requirement $V_{IL}(max)$ specification is too high to satisfy simultaniously the *maximum rise time* requirement, t_R. In this case the full SDA signal may be reconstituted using an external open-drain buffer as shown in Fig.6. The buffer isolates SDAOUT pin from the capacitance of the I²C-bus and makes the rise time requirement easier to meet.

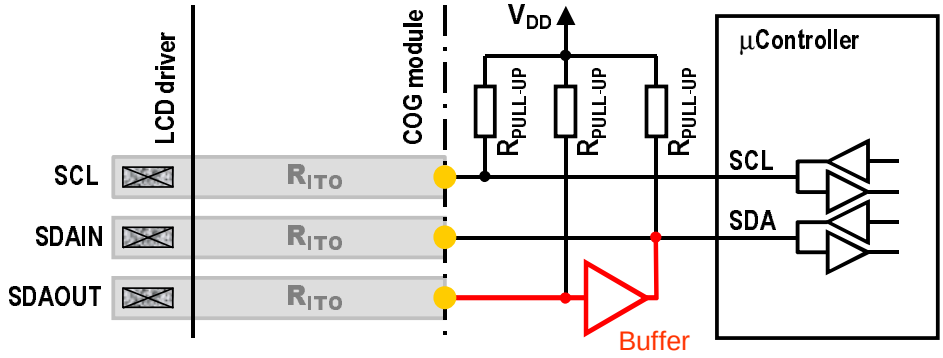

Fig.6 Connecting to a microcontroller via an open-drain buffer.

3) It is possible to implement the I²C protocol partially, in a way that ignores the ACKnowledge bit after each byte. SDAOUT may be left unconnected in this case, as shown in Fig.7. Such configuration may be desireable also because it eliminates the common-mode noise that results from the ACKnowledge current flowing through the common resistance in Vss supply of the driver IC. Note however that in this case any read-back function that is implemented in the LCD driver IC is not possible to use.

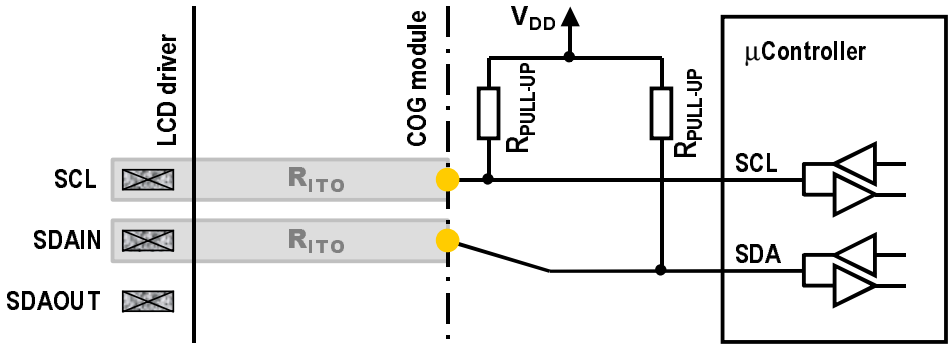

Fig.7 Example with SDAOUT pin left unconnected.

GUIDELINES FOR ESD/EMC PROTECTION

Dummy pads. Dummy pads must not be connected to ITO tracks. Connecting dummy pads may compromise ESD protection of the LCD module because these pads do not have ESD protection elements.

Harware RESET pad. In COG applications the interface and supply lines have higher impedance compared with COB, TCP, or COF. The resistance of individual lines may differ in value considerably from one ITO track to the next. This difference can be of the order of 100s of Ohm. As a result a large differential voltage can be generated across the ITO tracks during an EMC event. The RESET pad can recognise such EMI-induced voltage spike (of the order of 5 ns) as a reset command. To prevent this a low-pass filter is built into the RESET pad of most of the LCD driver ICs from Philips. However some older types require an external ITO resistor to be placed directly underneath the IC die, in order to create a first order low-pass filter together with the parasitic pad capacitance (as shown in Fig.8). These types are listed below:

PCF2119/F1 (but not PCF2119/F2), PCF8548/F1 & PCF8548/3, PCF8531/F1, PCF8801, OM6206 (but not OM6206/2)

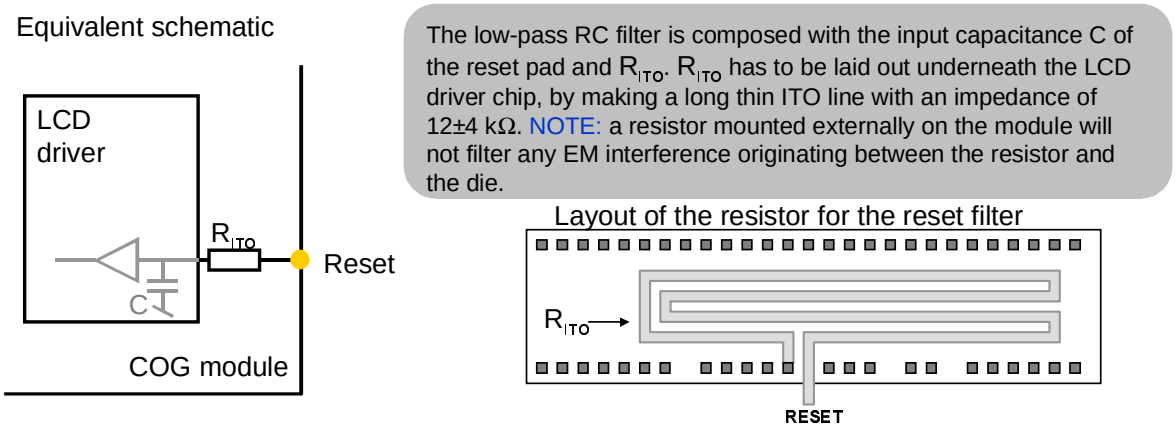

Fig.8 Implementation of ITO meander resistor for EMC low-pass filter.

Power supply tracks V_{SS}, V_{DD}. To increase EMC immunity further, it is recommended to reduce as much as possible the resistance of the ITO tracks and connections for power supply - V_{DD1}, V_{DD2}, V_{DD3}, V_{SS1}, V_{SS2}.

Unused pins - how to tie off. When pins are not used in the application (e.g. test pins, unused interface pins etc) it may be a requirement that these pins are tied to V_{DD1} or V_{SS1} (*tied off*). In this case it is important to make the connection to V_{DD1} or V_{SS1} as

direct as possible. Sometimes so-called *tie-off* pads are provided for this purpose (called Vxx1 TIEOFF or similar). If there are no tie-off pads then the connection must be made directly to V_{DD1} or V_{SS1} pads as shown in Fig.9.

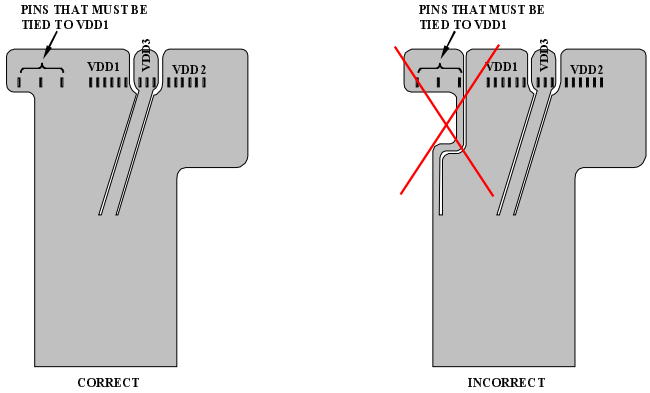

Fig.9 Tying off unused pins.